III. REMARKS

Claims 1-20 are pending in this application. Claims 1-11 are withdrawn from consideration. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Reconsideration in view of the following remarks is respectfully requested.

Entry of this Response is proper under 37 C.F.R. §1.116(b) because the Response: (a) places the application in condition for allowance as discussed below; (b) does not raise any new issues requiring further search and/or consideration; and (c) places the application in better form for appeal. Accordingly, Applicants respectfully request entry of this Response.

In the Office Action, claims 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al. (US Publication No. 2003/0183880), hereinafter "Goto," in view of Wolf, *Silicon Processing for the VLSI Era*, 1986, Volume I, pages 387 and 400, hereinafter "Wolf 1986," and Wolf, *Silicon Processing for the VLSI Era*, 1990, Volume II, page 146, hereinafter "Wolf 1990." Applicants respectfully submit that the claimed subject matter is allowable for the reasons stated below.

With respect to claims 12 and 20, for example, Applicants submit that the suggested combination does not disclose or suggest all the claim limitations. Specifically, the claimed invention includes, *inter alia*, "a silicide section positioned in one of a plurality of back-end-of-line (BEOL) layers[,] wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers[,]" as recited in claim 12 and claimed similarly in claim 20. As the Office admits, "[Goto] does not disclose using [*sic.*] a silicide resistor in a plurality of back-end-of-line layers with a silicidation temperature less than a damaging temperature of the BEOL layers[.]" (Office Action at page 2). Contrary to the

Office's assertion, however, Applicants submit that Wolf 1986 and Wolf 1990 do not overcome this deficiency of Goto because Wolf 1986 and Wolf 1990 do not disclose or suggest, *inter alia*, "a silicide section positioned in one of a plurality of back-end-of-line (BEOL) layers[.]" (Claim 12 of the claimed invention). The Office asserts, however, that "the resistor could be formed in any layer of the semiconductor device, including BEOL layers[.]" (Office Action at page 3). Applicants respectfully traverse this assertion because there is no suggestion or motivation to modify the two Wolf references in a manner to obtain the above-referenced feature. Wolf 1990 attempts to use the group III metals for "self-aligned ohmic contacts and local interconnects to silicon." (Wolf 1990 at 146, 2nd paragraph). As is known in the art, self-aligned ohmic contacts and local interconnects to silicon are in the first metal layer, which is by definition not one of a plurality of BEOL layers, as BEOL layers are formed on a semiconductor wafer in the course of device manufacturing following the first metallization.

In addition, Wolf 1990 only discloses that "[a]ll of the group VIII metals react with Si at 600°C or less" (Wolf 1990 at page 146), and Wolf 1986 only discloses that "silicides form [on Tungsten] at temperature > 600 °C" (Wolf 1986 at page 400). Such disclosures of the silicidation temperatures of the metals, without more, do not teach or suggest the claimed features. For example, both Wolf references do not disclose or suggest anything regarding damaging temperature of a plurality of BEOL layers; and both Wolf references do not disclose or suggest that a silicide section has a silicidation temperature less than a damaging temperature of a plurality of BEOL layers. Applicants submit that the absolute value of 600°C or less disclosed in Wolf 1990 is not equivalent to the relative temperature characteristic claimed in the claimed invention, i.e., a silicidation temperature less than a damaging temperature of the plurality of BEOL layers. Applicants submit that the Office is using the hindsight teachings of the claimed

invention to modify the Wolf references to obtain "a silicidation temperature less than a damaging temperature of the plurality of BEOL layers." (Claim 12 of the claimed invention). In addition, both Wolf references only disclose using the silicide materials for interconnect applications, not for a resistor application as claimed in the current invention.

In the Office Action, the Office asserts that "the silicidation temperature that ... are [*sic.*] less then a damaging temperature of a plurality of BEOL layers are defined in applicant's specification as 600°C or less[.]" (Office Action at pages 3-4). Applicants respectfully traverse this assertion because the specification of the current application, specifically paragraph 0020, provides the anneal temperature ranges of some illustrative examples of the metals that may be deposited on one of a plurality of BEOL layers, but does not define a damaging temperature of a plurality of BEOL layers as 600°C or less. The illustrative examples of the metals are provided for descriptive purpose only, but not to limit the scope of the claimed invention, including the scope of the damaging temperatures. Rather, the specification of the claimed invention clearly describes that "[f]or alternative BEOL wiring schemes that allow higher temperature processing, there are other material options for first metal 40[.]" (Paragraph 0021 of the current application). In view of the foregoing, the suggested combination does not disclose or suggest a silicide section having a silicidation temperature less than a damaging temperature of a plurality of BEOL layers.

In the Office Action, the Office asserts that "interconnects are, by definition, part of the back-end-of-line process." (Office Action at page 3). Applicants respectfully traverse this assertion because front-end-of-line layers also include interconnects. Moreover, Wolf 1990 only expects "interconnects to silicon", not the possible interconnects between BEOL layers because, as is known in the art, BEOL layers may include metal layers and dielectric layers, but do not

include silicon. In view of the foregoing, the suggested combination does not disclose or suggest, *inter alia*, "the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers."

Furthermore, Applicants submit that there is no suggestion or motivation to combine the cited references. Wolf 1990 and Wolf 1986 only expect to use the group III metals for forming contacts and interconnects to silicon, but not for forming a resistance element. (*See* Wolf 1990 at 146 and Wolf 1986 at 400.) As such, there is no motivation or suggestion to adopt the teachings of the Wolf references into Goto to form the resistance element. Applicants submit that the Office can obtain suggestion or motivation to combine the two Wolf references with Goto only from the hindsight teachings of the claimed invention, which is not warranted in a Section 103 rejection.

In view of the foregoing, the cited prior art references do not render the claimed invention obvious. Accordingly, Applicants respectfully request withdrawal of the rejection.

The dependent claims are believed allowable for the same reasons stated above, as well as for their own additional features.

Applicants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

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